Assessing Deep Reactive Ion Etch (DRIE) at CNF

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Cornell University's Nanoscale Science and Technology Facility (CNF) recently took delivery of a VERSALINE™ deep silicon dry etching system. The comprehensive assessment process described here took a year to complete.

Part of Cornell University in Ithaca, New York (U.S.A.), the Cornell NanoScale Science & Technology Facility (CNF) supports a broad range of nanoscale science and technology projects for users from academia, industry, and government laboratories. As an attractive alternative to setting up a nanoscale laboratory, the CNF is open 24 hours a day and provides state-of-the-art resources – including fabrication, synthesis, computation, characterization, and integration systems – combined with an expert staff to advise over 700 users that come every year (50% from outside Cornell).

The comprehensive tool set at CNF is particularly well suited to MEMS projects, with a team that has extensive experience and technology for polysilicon based MEMS as well as Silicon-on-Insulator (SOI) based and SiC MEMS. Users at CNF typically spend a week or two to complete their work. With the help of the expert staff, many projects are also carried out remotely. The range of MEMS projects done at CNF include:

- Accelerometers
- Sensors
- Inkjet heads
- RF switches
- Micro-fluidics
- Actuators

DRIE of silicon is a vital process technology in the fabrication of many types of micro-electromechanical systems (MEMS) devices. Fabrication of MEMS and other mechanical nanostructures is an active area within CNF, accounting for approximately 30% of the user base. Many of these application areas include optical MEMS, RF MEMS, biological MEMS, as well as integrated CMOS structures. DRIE enables the fabrication of high aspect ratio structures in silicon with anisotropic profiles and a high selectivity to the masking materials. DRIE, which utilizes a time division multiplex (TDM) process, in which alternating deposition and etching steps are used cyclically, has been part of CNF's process repertoire since the mid 1990's. This followed the SCREAM process, developed by MacDonald's group at CNF in the late 1980's, which used a chlorine-based process. CNF obtained one of the first TDM etching systems, a PlasmaTherm 770 in 1995, and in 1999 we obtained a second DRIE system, a Unaxis 770. Because the state-of-the-art in deep reactive ion etching continues to advance rapidly, CNF wanted to upgrade its DRIE capability in order to best serve its growing base.

A yearlong process

In order to procure the best R&D-based DRIE system available, CNF initiated a comprehensive assessment of four major vendors with an established history of accomplishment in this field. This yearlong assessment began in mid 2006 and concluded in the late spring of 2007. Unlike in industry, where the search for a tool is based on the production of one or two devices, CNF's toolset must meet the objectives of its many users and diverse projects. Hence, this system must not only demonstrate outstanding performance, but must have a very large process window for versatility in its many applications.

CNF believed that the best way to accurately assess the overall performance of a system was by generating a design of experiments (DOE). The range of the DOE was based on a preliminary discussion between CNF and process engineers. The design was based on an orthogonal Taguchi L9, with 4 process factors and 3 level settings for

each input parameter. The input parameters chosen for the Oerlikon VERSALINE™ system included RIE peak-to-peak bias voltage, ICP source power, pressure, and C_4F_8/SF_6 flow settings. Other relevant parameters such as the deposition pressure and the respective cycle times were fixed.

The output metrics were etch rate, selectivity to both photoresist and silicon dioxide, %RIE lag, and overall profile evolution. Eighteen 4-inch wafers were prepared with equal numbers of resist and oxide masked wafers. The reticle used to pattern these wafers was designed to incorporate a large variety of geometric features and sizes.

Run	Gas (C_4F_8/SF_6)	Etch A Bias (V_{p-p})	Etch B ICP (W)	Etch B Pressure (mTorr)
1	100/300	100	2000	50
2	200/450	400	2500	70
3	300/600	400	3000	90
4	300/600	500	2000	70
5	100/300	500	2500	90
6	200/450	500	3000	50
7	200/450	600	2000	90
8	300/600	600	2500	50
9	100/300	600	3000	70

Large area grating structures composed of a large range of lines and spaces from submicron to 50µm in dimension were used. These structures were used to investigate micro and macro loading effects as well as to examine RIE lag, also known as aspect ratio dependent etching (ARDE). The pinwheel structures offered an effective means to evaluate sidewall morphology. The wafer design consisted of many die to allow for efficient post processing characterization and SEM cross sectioning.

An ideal solution

The VERSALINE™ system incorporates Oerlikon's latest Deep Silicon Etch (DSE®) technology and provides the etching precision and process latitude necessary to create next generation nanoscale and MEMS devices. This platform has successfully integrated several process technologies that enable sub-second etch and deposition steps for DSE. Sub-second switching between process steps produces smooth sidewall profiles as scalloping is reduced to a minimum. A patented fast gas switching technique using solenoids coupled with mass flow controllers, is only one of several components for high performance, fast response processing. Pressure control technology commensurate with the changes in gas flow is accomplished using a combination of high speed throttle valves and patented control algorithms.

The challenge of maintaining inductively coupled plasma performance in a fast changing environment is met by utilizing a solid state matching network. This solid state matching technology not only ensures efficient impedance matching and power transfer to the plasma on a sub-second timescale, but also eliminates the mechanical wear encountered with traditional motorized matching networks. Another important technology enabling sub-second deep silicon etching processes is endpoint control. A highly sensitive optical emission spectroscopy system (OES) developed by Oerlikon is used with patented endpoint algorithms to compliment SOI etch capability. These technologies result in overall process speeds approaching the system's limit of gas residence time.

Although not addressed in this evaluation, Oerlikon provides a unique SOI solution to notching at the silicon/buried oxide interface. Electrode bias includes the ability to select an arbitrary waveform for charge relaxation and provides flexibility that can be tailored to specific SOI structures.

When combined with dedicated microprocessors, the system leverages fast gas switching, rapid response pressure control, immediate plasma power matching, and sensitive endpoint detection to produce a complete, enabling advance in deep silicon etching. This advance promotes both innovation and commercialization in the emerging markets of MEMS, nanotechnology, and packaging.

DOE trends of silicon etch rate, selectivity to oxide and resist masks, and RIE lag

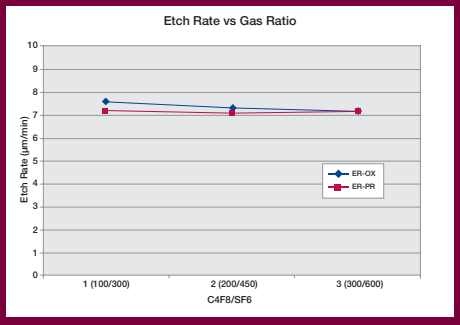


Figure 1.

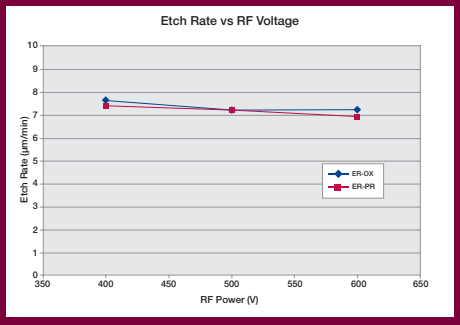
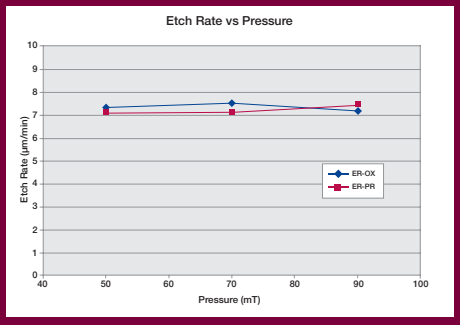


Figure 2.



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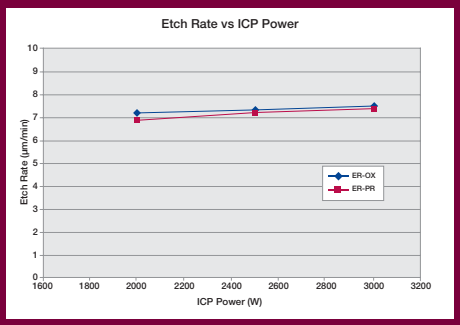


Figure 4.

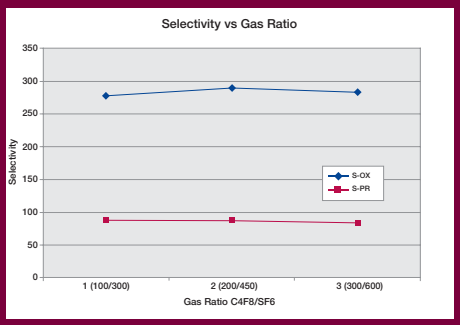


Figure 5.

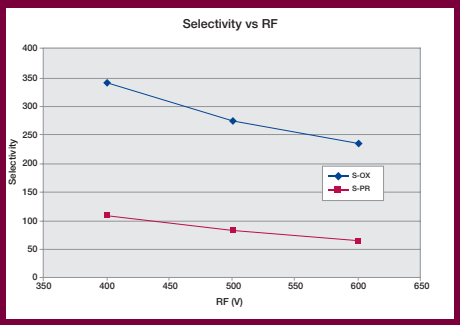


Figure 6.

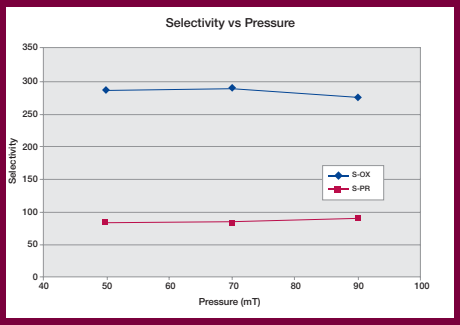
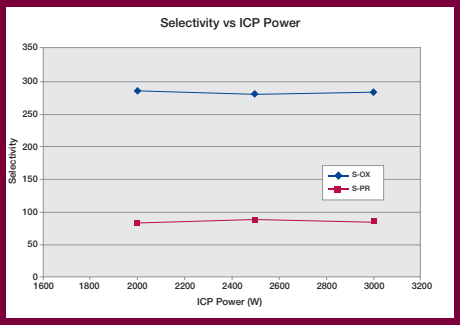


Figure 7.



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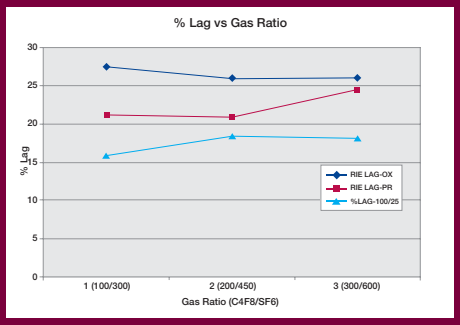

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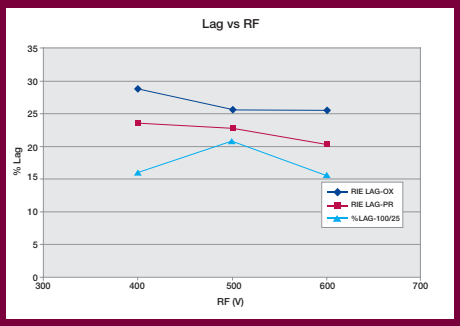

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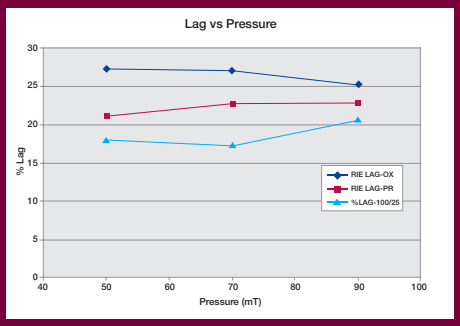

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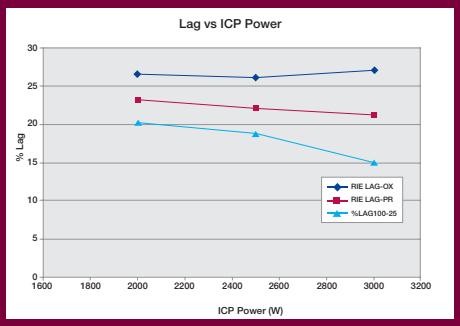
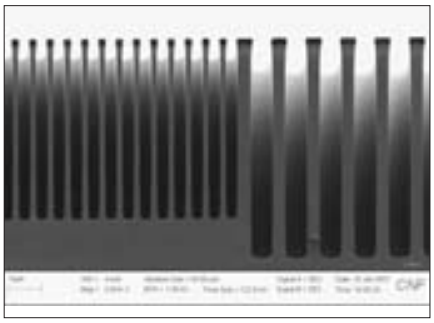


Figure 12.

Figure 13. Run 3 conditions with a resist mask depicting 2.5µm and 5µm features with a selectivity of 111:1 and an etch rate of 8µm/min



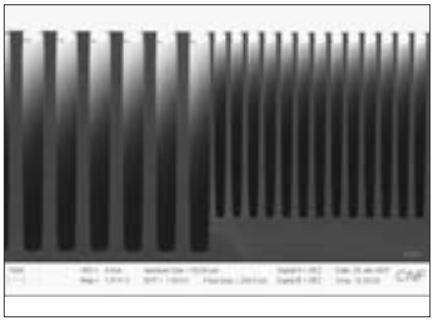
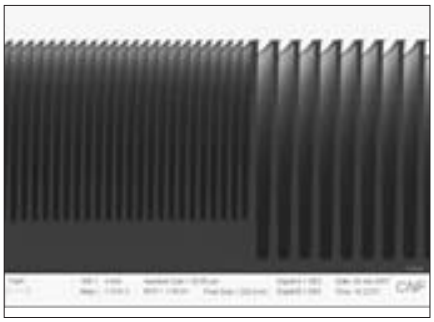


Figure 14. Run 3 conditions with an oxide mask depicting 10µm and 5µm features with a selectivity of 340:1 and an etch rate of 7µm/min

Figure 15. Run 4 conditions with an oxide mask depicting 2.5µm and 5µm features with a selectivity of 333:1, an etch rate of 7µm/min and an aspect ratio of 35:1



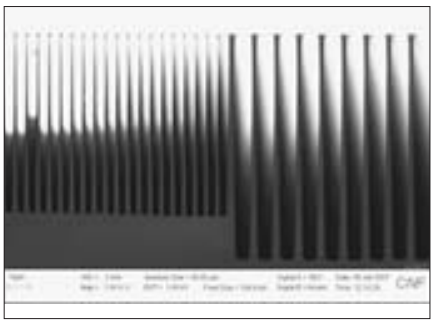


Figure 16. Run 7 conditions with an oxide mask depicting 2.5µm and 5µm features, an etch rate of 7µm/min and an aspect ratio of 33:1

DOE Results

The results of the DOE performed on the VERSALINE™ system were analyzed by obtaining the average value of the outputs as a function of the input variable over the specified ranges. The etch rates consistently averaged between 7-8µm/min with respect to RIE bias, ICP power, pressure, and C_4F_8/SF_6 (see Figures 1-4). All four of the input parameters appear to have an equal influence on the etch rate. These high etch rates which are consistent throughout the normal parameter space are indicative of a very advanced ICP design that maximizes the dissociation of SF_6 into a large concentration of atomic fluorine that is largely responsible for etching.

The selectivities achieved with respect to both photoresist and silicon oxide masks were outstanding over the entire process window, as illustrated in Figures 5-8 and in the SEM micrographs (Figures 13 & 14). Selectivity to photoresist (non-hard baked) was consistently 85-90:1 and as high as 110:1. Selectivity to silicon oxide averaged 275-290:1 and was measured as high as 340:1. Achieving these high selectivities simultaneously with high etch rates is due to application of a unique RF strategy in which bias is only applied during the depassivation etch step (etch A) and not during the isotropic silicon etch (etch B) which only consists of ICP power. This is supported by the data, which indicates that RF bias voltage had the largest influence on selectivity.

RIE lag, which is the disparity in etch depth as function of feature size, was measured across the DOE in which the etch depth of a low aspect ratio feature is normalized to that of a 50µm feature, as illustrated in Figures 9-12). The etch depth of these features varied by only 22% on average. This excellent result is achieved without employing any techniques such as higher pressures and flows, or the addition of O_2. RIE lag is normally caused by the depletion of reactive neutrals and ions in higher aspect ratio features. These results are again indicative of a very sophisticated plasma reactor design.

The ability to etch features of high aspect ratio is extremely important in both MEMS and microelectronic fabrication. This was clearly demonstrated within the parameter space of the DOE. As illustrated in the accompanying SEM micrographs (Figures 15 & 16), feature widths of 2.5µm were etched to an aspect ratio of 35:1, without any indication of sidewall bowing which ultimately leads to etch termination. With continued processing, we are confident that aspect ratios of at least 50:1 are achievable, again without any process enhancements.

Sidewall morphology of a TDM process is typically characterized by scalloping due to the cyclic nature of the process. The depth of the scallops is largely a function of the etch cycle time and can be reduced by decreasing the etch step time with the assistance of fast switching MFCs. The silicon etch step time for the DOE was 2 seconds, and the depth of the scalloping was only 0.05µm, yielding an impressively smooth sidewall. Using the fast switching MFCs on the VERSALINE™ with subsecond etch cycle times will generate sidewalls that are significantly smoother.

Outstanding process latitude

Perhaps the most important and impressive result of the VERSALINE™ assessment was the outstanding process latitude demonstrated for each of the input variables over the selected ranges. Having a tool demonstrate this level of process stability is the desire of every process engineer. In addition, achieving high etching rates and selectivities with this range of process latitude is extremely noteworthy.

The results of the VERSALINE™ assessment clearly surpassed the competition and achieved all the objectives put forth by CNF. The high figures of merit along with outstanding process latitude allow CNF to meet and surpass the requirements of its many users and diverse projects. This state of the art system will allow CNF to advance all aspects of MEMS technology for many years to come.

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