The Effects of Increasing the Aspect Ratio of GaAs Backside Vias

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Keywords: GaAs Etch, slot vias, Aspect Ratio Dependent Etching, Via density

Abstract

To support the current trend in industry of working towards higher via densities which could shrink via dimensions, we report new process development work to accommodate these smaller via geometries.

INTRODUCTION

GaAs is widely used throughout the wireless telecommunications industry in the manufacture of devices such as high electron mobility transistors (HEMTs). While this material system has excellent electrical properties that lends it well to applications requiring high-efficiency and/or high-frequency operation, this intrinsic performance advantage also requires maintaining low extrinsic parasitics such as ground inductance. A common strategy employed throughout the industry for reducing the effect of this parasitic is the use of through-substrate vias also commonly referred to as backside vias. For frequencies of operation at X-band and above it is common practice to employ transistor designs featuring source contacts that are individually connected to through substrate vias. These vias, often referred to as slot vias[1], can result in very low overall circuit inductance by reducing the lead inductance component of this parasitic, but the approach requires vias of exceedingly small lateral dimension and high aspect ratio. Such reduced dimension vias are also proving enabling to further die shrink for more cost sensitive applications. Consequently, the trend in the industry has been toward higher via densities and shrinking via dimension. While traditional vias have relatively modest aspect ratios (typically 1.7 – 2.5:1), emerging slot via designs are approaching aspect ratios approaching 10:1. Although reducing via geometry may offer significant advantages, it also presents a unique set of process challenges to photoresist patterning, etch throughput and quality, as well as reliable metallization of these vias. In this paper, we present the results of process development work targeted to address these emerging geometries.

In papers previously presented in this conference we reported pillar free GaAs via etch processes with etch rates greater than 10µm/min for vias with aspect ratios of less than one[2,3]. This paper will report etch rates for high aspect ratio slot vias. For aspect ratios as high as 10, in a 5µm x 10µm square slot via etched to a 50µm depth, we are reporting etch rates of 3 um/min. This is a vertical via, with smooth sidewalls, as shown in Figure 1.

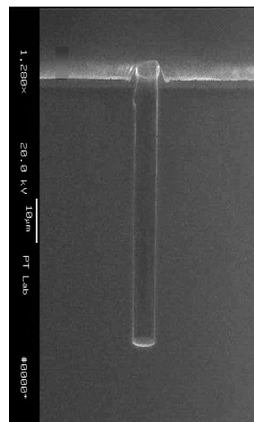

FIGURE 1: The 5µm side of a 5µm x 10µm slot via etched to a 50µm depth (10:1 AR).

The process regime for the high aspect ratio via result shown in Figure 1 has been characterized using a designed experiment. The process parameters varied in this study were pressure, total gas flow, bias power, and ICP power. The responses analyzed include GaAs etch rate, photoresist etch rate, selectivity, and sidewall quality. One of the challenges associated with etching GaAs at high etch rates or at high aspect ratios, is maintaining smooth sidewall quality. We will report in this paper how the selectivity of the GaAs to the photoresist mask correlates to the quality of the sidewall morphology of the vias. We will also present plating uniformity data of the slot vias. Finally, a study involving the effect of via spacing and density, and their effect on plasma loading will be summarized and presented.

EXPERIMENTAL

All wafers were etched in a Plasma-Therm, LLC Versaline™ ICP etcher. This system features a 2MHz ICP source and 13.56MHz independently biased cathode. Wafer

temperature was controlled by electrostatically clamping the wafer to a cooled cathode with helium backside cooling.

The substrates used in these experiments were 100mm, full thickness, mechanical GaAs wafers patterned with a photoresist mask. The effective open area of GaAs due to the vias was less than 10%.

All GaAs etch depth measurements were taken from vias at the center of the wafers. These measurements were performed using an Amray Scanning Electron Microscope model 1830. A Nanometrics NanoSpec model 6100 spectroscopic reflectometer was used to measure the photoresist thickness. Twenty-five sites on each wafer were measured before and after etch, with an edge exclusion of 6mm. An average of the 25 point measurement was used in the calculations of photoresist etch rate and selectivity.

The DOE to characterize the process space was setup and analyzed using Design Expert software from Stat-Ease, Inc. An irregular fraction design was utilized to construct the experiments covering 4 factors in 12 experiments with 3 repeats of the center point for 15 total experiments. An irregular fraction allows the estimation of the main effects as well as 2 factor interactions. The effects of these factors were characterized through the four captured responses: GaAs etch rate, photoresist etch rate, selectivity, and via sidewall quality. Total etch time, process temperature, and hardware configuration were held constant throughout these experiments.

The sidewall quality of the vias was evaluated after a photoresist strip in an acetone bath. Cross-sectional SEM images of these vias were presented to several engineers for a numerical evaluation of the quality. The average of these ratings was used as the response.

RESULTS AND DISCUSSION

A) *Designed Experiment*

In Table I, the general response trends from the DOE are summarized. The arrows indicate the directional change in the response resulting from an increase in the listed process factor.

TABLE II
GENERAL RESPONSE TRENDS FROM DOE

		Responses			
Factors		GaAs Etch Rate	Photoresist Etch Rate	Selectivity (GaAs:PR)	Sidewall Quality
	Pressure ↑	↑	↓	↑	↓
	Cl_2 Flow ↑	↑	↑		↓
	Bias Power ↑		↑	↓	
	ICP Power ↑		↑	↓	

Increases in GaAs etch rate are shown to be directly related to increases in pressure and total Cl_2 gas flow. Reducing the total flow at constant pressure or reducing the total flow at higher pressures leads to longer residence times for the reactants. Longer residence times give the available reactants more time within the system to react with the etch surface. The residence times in this DOE ranged from 0.45 seconds to 2 seconds.

Photoresist etch rate increases with increasing bias and ICP powers. This can be attributed to an increase in power density at the wafer. The increase in photoresist etch rate due to Cl_2 gas flow can be attributed to a higher concentration of Cl available to react with the photoresist. The highest photoresist etch rates occurred at the lowest pressures, highest Cl_2 flows, and highest powers investigated. Figure 2 shows the dependence of photoresist etch rate on Cl_2 flow and pressure at a given power level. Consequently, selectivity decreased with increasing powers due to the photoresist etching considerably faster at higher powers. Also, there is a direct relationship between pressure and selectivity. As pressure increases, so does selectivity.

A summary of the rating system used to evaluate the sidewall quality of the vias is described with Figure 3. An interaction of factors was observed when looking at the response of sidewall quality of the vias. At higher Cl_2 flows, sidewall quality decreases with increasing pressure. But at lower Cl_2 flows, sidewall morphology is smooth and independent of pressure changes in the factor range investigated, as shown in Figure 4. This could be attributed to a reactant limited scenario at the lower flows.

Figure 5 illustrates the correlation drawn between selectivity and the quality of the sidewall morphology of the vias studied. It was found that the smoother sidewall morphology of the vias occurred at the lower selectivities. This would indicate that more photoresist-based polymer is being produced at the higher photoresist etch rates, to better protect the sidewalls of the vias.

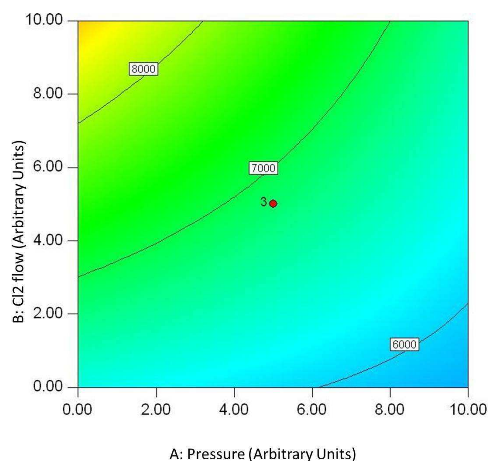

FIGURE 2: Interaction effects of pressure and Cl_2 flow on photoresist etch rate (Å/min). High photoresist etch rates (Å/min) occur at low pressures and high Cl_2 flows.

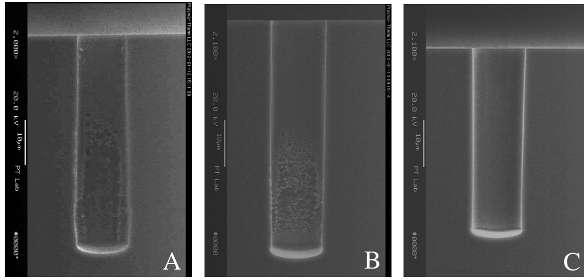

FIGURE 3: Examples of via images used in the sidewall quality evaluation. The engineers surveyed assessed only the sidewall morphology. They were given the scale of 1 representing many sidewall voids and 10 representing a via with very smooth sidewalls. The average rating of via A was 2.5, via B was 4.5, and via C was 10.

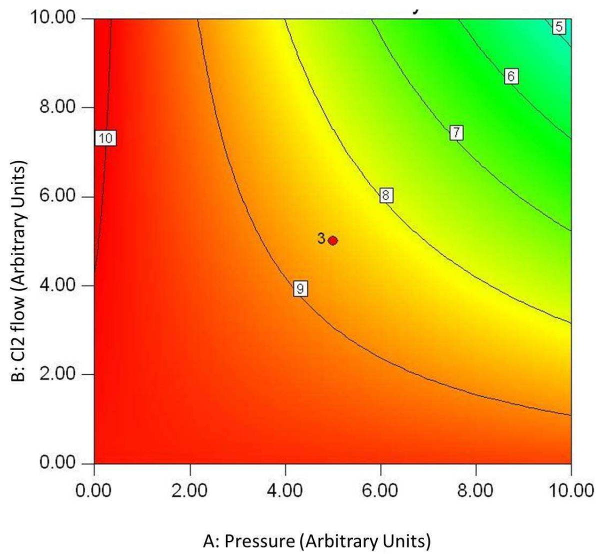

FIGURE 4: Interaction effects of pressure and Cl_2 flow on sidewall quality. Sidewall quality scale with a 1 represents a via with a lot of sidewall voids and a rating of 10 represents a via with very smooth sidewalls. At higher Cl_2 flows, sidewall quality decreases with increasing pressure. At lower Cl_2 flows, sidewall quality is independent of pressure.

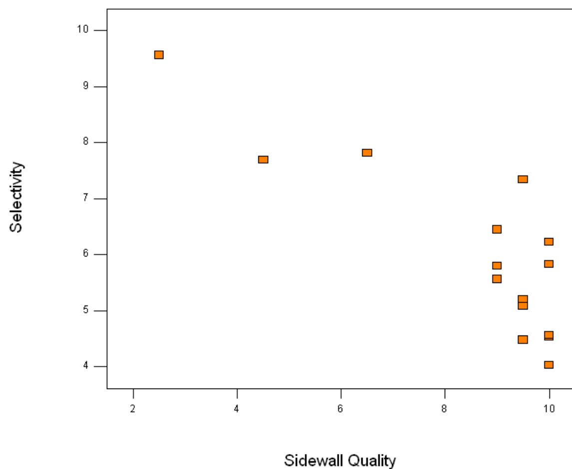

FIGURE 5: Correlation of Selectivity to Sidewall Quality, the higher the selectivity the lower the sidewall quality.

B) Aspect Ratio Dependent Etching of Slot Vias

We are also presenting the aspect ratio dependent etch rate data for slot vias. This topic has been studied in the past for a RIE only process[4]. This work presents an extension of that curve using an ICP process.

If A defines the radius of the via in the x-direction and B defines the radius of the via in the y-direction. When A=B, the vias are circular and the aspect ratio (AR) is defined to be the ratio of the etch depth (D) to the diameter of the via (2*A = 2*B). For slot vias, when A < B, then the aspect ratio (AR) is defined as AR = D / 2*A.

The center point process of the DOE was used to generate the data in the curve presented in Figure 7. The etch rate data is a time based average. The same process was used and the etch depth was measured at 2 minute intervals of the etch. This was done to assess how fast the etch depth increased over time. These vias were all grass free and showed smooth sidewalls. Five different slot via sizes were measured and plotted on the curve, ranging from 20 x 25µm vias to 20 x 5µm vias. We are reporting the capability to etch 10 x 5µm slot vias to more than a 50µm etch depth with smooth sidewalls, as seen in Figure 1. This gives a greater than 10:1 aspect ratio via etched at more than 3µm/min.

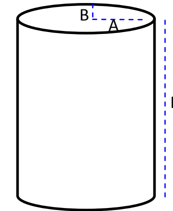

FIGURE 6: Illustration depicting slot via dimensions, where A is the radius in the x-direction, B is the radius in the y-direction and D is the total etch depth.

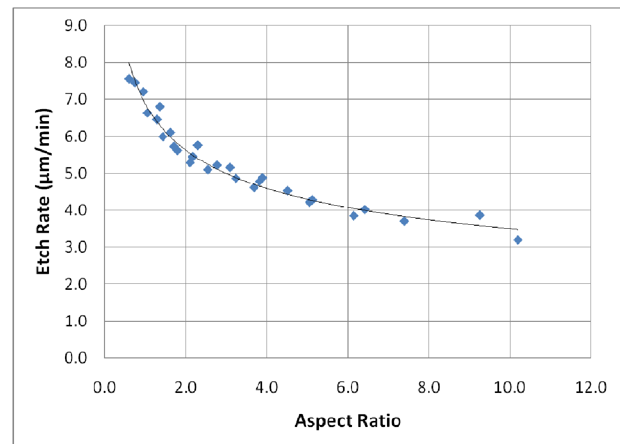

FIGURE 7: Time averaged etch rate as a function of aspect ratio for slot vias, from 20x25µm to 20x5µm slot vias.

C) Plating Uniformity

Also presented are the results of a test reticle created for these studies that features vias of various size and density that was used to quantify etch and plating system interactions. A series of via sizes ranging from 15x5µm to 15x30µm from the test reticle are shown in Figure 8A. Figures 8B and 8C illustrate the extent of plated taper present in the process – metallization thickness was found to consistently maintain approximately 85% of its nominal value from back to front. Overall, excellent plating uniformity was obtained for all via geometries in this series.

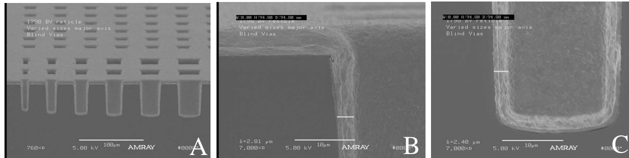

FIGURE 8: Figure 8A shows a series of via sizes ranging from 15x5µm to 15x30µm. Figure 8B shows the gold on the sidewall at the top of the via to be 2.8µm thick. Figure 8C shows the gold on the sidewall at the bottom of the via to be 2.4 µm thick.

D) Study of Via Spacing and Density

A study involving the effect of via spacing and density and their effect on plasma loading was also conducted. A series of 10 x 20 µm Vias with varying pitch in X and Y directions in 12 distinct pads was created from a sparse via density of 80 vias, to a high density of 240 vias.

The center-point of the triplicate run (from DOE) wafer was selected for analysis. The variations in diameter, and depth of the vias etched in the various X and Y pitches and densities from 80 vias (the most sparsely populated array) to 240 vias (most densely populated array) was remarkably low at 1 sigma<2.5%. The angle of the straight wall of the vias was always 88.5 degrees or greater. Figures 9 and 10 show the cross-section images for the sparsest and densest arrays, for both the major and minor axes. The vias etched uniformly and consistently regardless of spacing or density. This shows that there is a no loading effect based on the via spacing and density investigated for the center-point process of the DOE presented earlier.

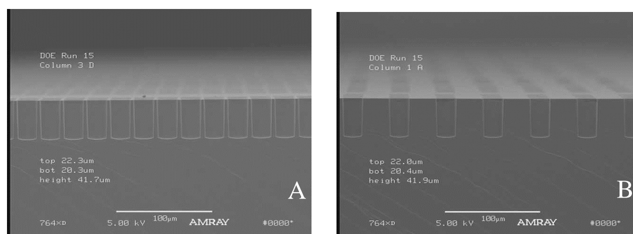

FIGURE 9: Figure 9A shows the major axis for most densely packed array of vias. Figure 9B shows the minor axis of the most densely packed array of vias.

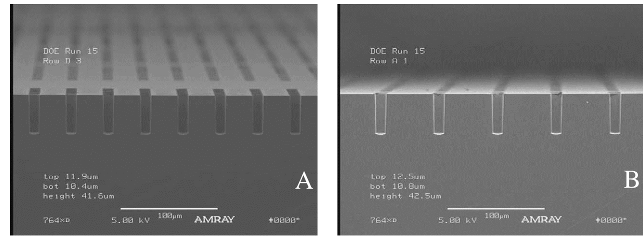

FIGURE 10: Figure 10A shows the major axis for sparsely packed array of vias. Figure 10B shows the minor axis of the sparsely packed array of vias.

CONCLUSIONS

In this paper, we are reporting GaAs etch rates greater than 3µm/min for slot vias with aspect ratios of 10:1. These vias were etched with vertical profiles and smooth sidewalls. The process regime for these studied through the use of a DOE. It was found that GaAs etch rates increase with increasing pressure and total gas flow. Though the average etch rate of the slot vias studied in this DOE are slow, compared to the previously presented work, this is due to their much higher aspect ratios. It was also found that selectivity increases as pressure increases. There is a direct correlation between sidewall quality and selectivity. The higher the selectivity gave lower sidewall quality, vias with more voids in the sidewalls. This highlights a potential tradeoff when trying to increase the GaAs etch rate while maintaining smooth sidewall morphologies.

ACKNOWLEDGEMENTS

The authors would like to thank those who prepared the samples, assisted in mask design, supported wafer fabrication and processing, as well as those who provided technical support for the etch chamber during the course of this work.

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ACRONYMS

HEMT: High Electron Mobility Transistors
ICP: Inductively Coupled Plasma
DOE: Design of Experiment
Cl_2 : Chlorine
GaAs: Gallium Arsenide