

Notch Reduction in Silicon on Insulator (SOI) Structures Using a Time Division Multiplex Etch Process

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Abstract

Silicon on Insulator (SOI) substrates are being increasingly used in MEMS applications, with the insulating layers serving as etch stop/sacrificial layers and/or device function layers. Apart from the conventional etching requirements including high etch rate, high selectivity and smooth sidewall, satisfactory etching of SOI wafers requires no notching at the silicon/insulator interface. Notching results from electrical charging effects and the consequent bending of the trajectories of arriving ions into feature sidewall. Notching is also aggravated due to the aspect ratio dependent etching effect.

At Unaxis USA, we have developed a proprietary technique to alleviate the problem of notching. This technique is integrated into Unaxis' advanced DSETM III silicon etching technology. A conventional time division multiplexed process is used during the bulk etch process while a proprietary finish etch process is used to eliminate notching. The transition between the bulk etch process and finish etch process is enabled using an advanced optical emission end point technique. The finish etch process is characterized and notch performance is measured as a function of overetch percentage and feature aspect ratio. Using this technique, notching is completely eliminated in aspect ratios of 8:1 and lower and reduced to less than 200 nm for aspect ratios up to 25:1.

1.0 Introduction

Deep silicon etching (DSE) is increasingly involved in Micro-Electro-Mechanical Systems (MEMS) applications, which often require fabrication of high aspect ratio features in silicon substrates. The DSE processes with perhaps the most widespread industrial use are those referred to as being Time Division Multiplexed (TDM). In principle, a TDM process cyclically alternates between etching and deposition cycles to generate anisotropic structures. For example, in an inductively coupled plasma (ICP) dry etching chamber, SF₆ chemistry is used in etching cycles and C₄F₈ is used in deposition cycles.^{1,2} A TDM process needs to satisfy many processing requirements, including high etching rate, smooth sidewall, high selectivity to mask materials and minimal lateral mask undercut.³

Certain MEMS applications also require that a silicon substrate be etched down to an insulating layer, which serves as an etch stop or as a device function layer. Thus MEMS device fabrication is increasingly turning towards silicon-on-insulator (SOI) wafers. In its simplest forms, a SOI wafer often has a layer of single crystal silicon atop an oxide layer which is deposited either through thermal oxidation, PVD, CVD, or PECVD or even simpler, the silicon wafer is bonded to glass. In more complex designs, an insulating layer can be “buried” between silicon layers.

When SOI wafers are etched using a TDM process a well-documented phenomenon, commonly referred to as “notching”, occurs.^{4,5} This is evidenced as a localized undercutting of silicon at the silicon/insulator interface, as shown in Figure 1(a). It is generally understood that electrical charging effects are responsible for notching. The charging effects are not present during bulk etch because the silicon substrate is sufficiently conductive to ensure that current flow within the substrate prevents any charge separation (see Figure 1(b)). However, when the etch front reaches the silicon/insulator interface, the insulator is exposed and the conductive current path is broken, allowing charge separation to occur. Because of the different angular distributions of ions and electrons in the plasma, positive ions tend to accumulate at the bottom of the feature, and electrons at the top. The resultant electric field is strong enough to bend the trajectories of arriving ions into the feature sidewall where lateral etching (notching) occurs, as shown in Figure 1(c). In many MEMS device applications, the notch formation is very undesirable.

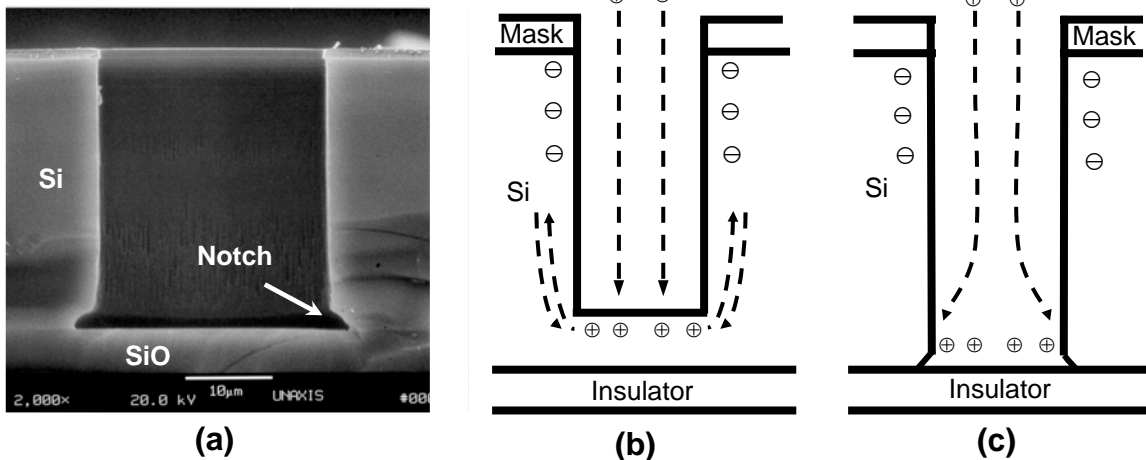


Figure 1: (a) Notching at Si/oxide interface in a conventional DSE etch process, (b) current flow within Si substrate prevents charge separation during bulk etch, and (c) charging effects causes notching to occur in the overetch period.

Notching becomes aggravated by the aspect ratio dependent etching (ARDE) effects. In ARDE, mass transfer of reagents and reaction products result in wider features being etched faster and reaching the insulating layer faster than the narrower features. Therefore, wider features have to be over-etched in order to etch all the narrower features to the same depth. Usually, “overetch” on a cleared feature is described as the percentage of overall process time it is exposed to the plasma while the narrower features are still being etched. It is during this overetch period when

charge accumulation and separation, and hence notching, occur in the already cleared features. In fact, due to ARDE and the range of features sizes on a wafer, overetch percentage sometimes can be as high as 60 %. Also, the aspect ratio determines the extent to which notching occurs. In general, notching becomes more severe as the aspect ratio increases.

Notching at the silicon/insulator interface is also more prevalent in high-density plasma, because the ion density is greater. The effect can therefore be reduced by the use of a low-density plasma which is employed only after the insulator has been exposed.⁶ However, the major drawback of such an approach is the low etch rate attainable.

2.0 Unaxis DSE III™ solution for SOI

The problem of charge effects and notching in conventional DSE processes has prompted Unaxis Wafer Processing to develop a proprietary method to significantly reduce and, in certain cases, completely eliminate notching. This method is developed on the Unaxis DSE™ III platform and requires the etching process to be divided into two parts as illustrated in Figure 2(a). The bulk of the silicon in the SOI wafer is etched with a conventional DSE process (t_1), which produces smooth sidewall at high etch rate, high selectivity to mask, and minimum mask undercut. The second part is a “finish” etch process that is utilized to etch the narrower features and is equal to the overetch period t_3 . The dry etching of silicon is carried out by generating high-density plasma using an ICP source operated at 2 MHz. The wafer is electrostatically clamped to an electrode with He backside cooling. An independent RF bias is supplied to the electrode to control bias voltage.

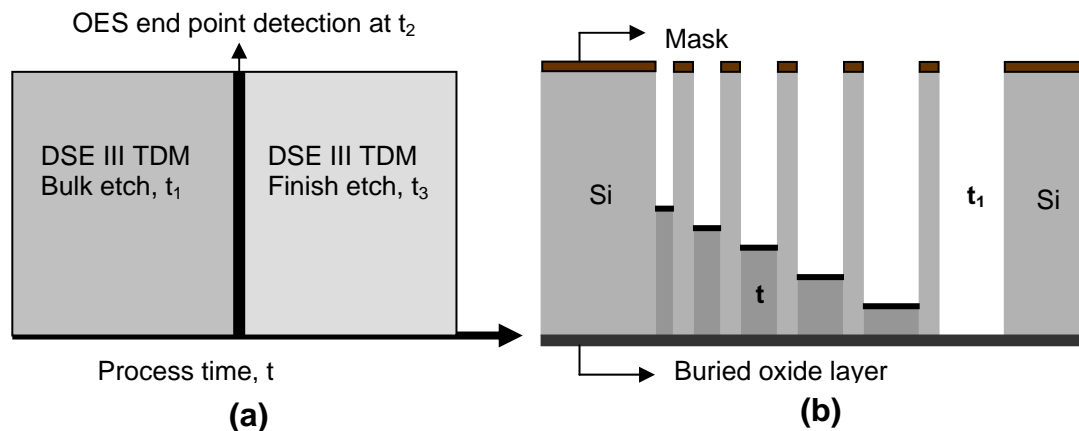


Figure 2: Process schematic showing DSE™ III bulk etch and Unaxis proprietary DSE™ III finish etch.

A critical component of this hybrid process is the transition between the bulk and finish etch steps. Since notch formation is sensitive to the overetch percentage, any significant exposure of the oxide layer to plasma during t_1 will cause notching. In order to make the timely transition, a Unaxis' optical emission spectroscopy (OES) system is used to detect the initial exposure of the oxide in the widest features. This is t_2 in the Figure 2. With Unaxis OES endpoint algorithm uniquely programmed for TDM processes, exposed oxide in the lowest aspect ratio features is detected at as little as 2% open area on a 150 mm silicon wafer.

As illustrated in Figure 2(b), the etch depth in the various features depends on the feature width. The feature on the far right is almost entirely etched using the bulk etch process. The OES end point algorithms first detect when the features equivalent to the far right feature is cleared throughout the wafer, and then trigger the transition to the DSETM finish etch step to clear the unetched silicon in the higher aspect ratio features. Figure 2(b) highlights the transition from the bulk etch step to the finish etch step with respect to the different features. Using this hybrid process, notching at the Si-oxide interface is greatly reduced. In essence, Unaxis finish etching process technology compensates for the conditions that lead to notch formation, namely, positive charge accumulation on the buried oxide surfaces.

The SEM image in Figure 3(a) is a cross-section of a standard Unaxis SOI test structure etched with this hybrid DSETM SOI process. The insulating SiO₂ layer has a thickness of 1 μm and is buried in two layers of single crystal Si. The aspect ratios range from 22:1 to 5:1 for the 50 μm-deep features. As seen, the notching is completely eliminated for features with aspect ratios of 8:1 and lower. By using this hybrid process for SOI wafers, significant overetching of the smaller aspect ratio features is possible. Even with significant overetching, notching is not seen on features with aspect ratios of 5:1 and lower. This is illustrated in Figure 3(b) with a high-magnification SEM image of the silicon/oxide interface on a 5:1 aspect ratio feature.

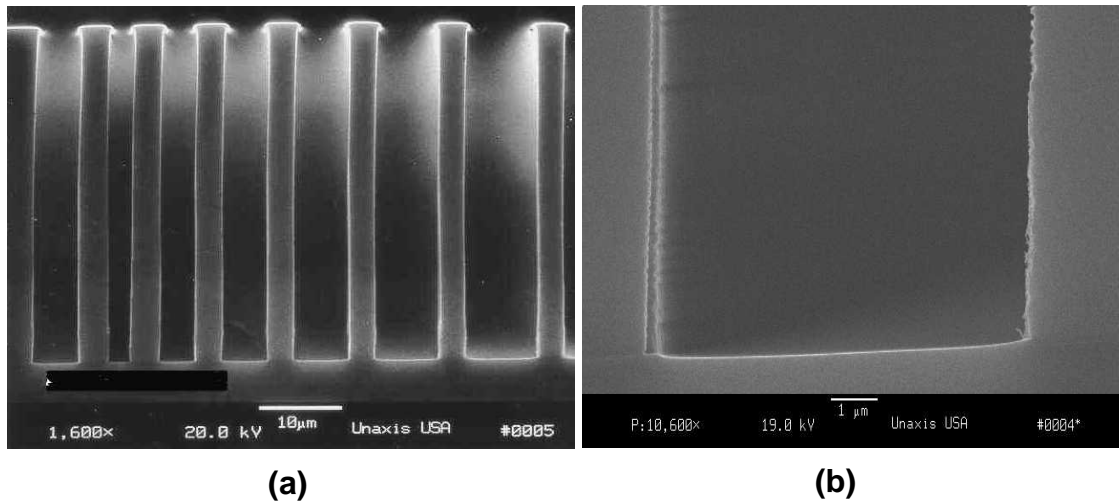


Figure 3: Notch reduction with Unaxis proprietary DSETM III finish etch.

The finish etch process is characterized and the notch reduction performance is measured as a function of overetch percentage and feature aspect ratio. The results are summarized in Figure 4 below. Using the Unaxis proprietary DSETM etch technique, notch is completely eliminated in features with aspect ratios up to 8:1. Even with up to 60% overetch, silicon features with aspect ratio of 5:1 remain notch-free. For features with aspect ratios up to 25:1, the notch is reduced to below 200 nm under extended overetch.

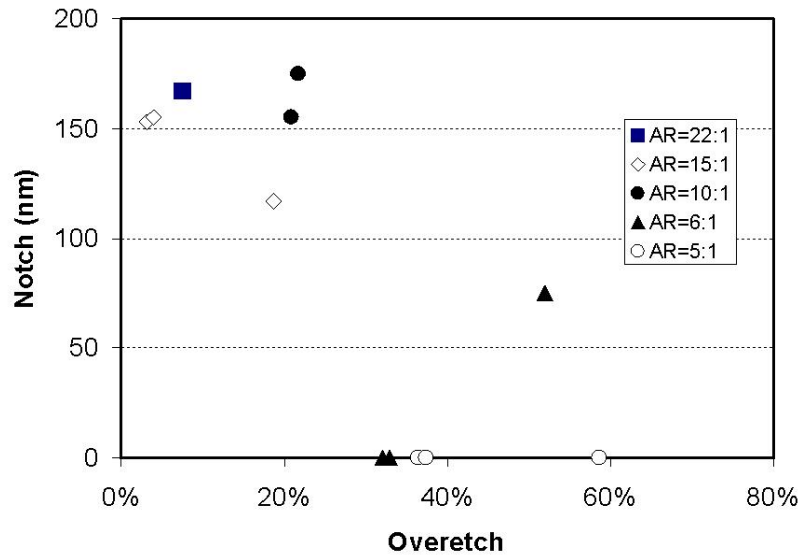


Figure 4: Notch reduction performance as a function of overetch percentage and feature aspect ratio.

3.0 Conclusions

The emerging importance of SOI substrates for MEMS processing is the driving force behind the Unaxis DSE™ III SOI hybrid process. The opportunity for MEMS designers to incorporate SOI structures in their devices requires eliminating notching without sacrificing etching rate, sidewall smoothness, profile quality, or mask selectivity. Recent progress at Unaxis maintains the advantages of using high-density plasma for high-rate deep silicon etching. A two-step hybrid etch process that relies on sensitive endpoint detection and charge dissipation effectively reduces notch formation. Notching is completely eliminated in aspect ratios of 8:1 and lower and reduced to less than 200 nm for aspect ratios up to 25:1.

4.0 References

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